

A new perspective for modeling power electronics converters: complementarity framework

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Abstract— The switching behavior of power converters with ‘ideal’ electronic devices (EDs) makes it difficult to define a switched model that describes the dynamics of the converter in all possible operating conditions, i.e. a ‘complete’ model. Indeed simplifying assumptions on the sequences of modes are usually adopted, also in order to obtain averaged models and discrete-time maps. In this paper we show how the complementarity framework can be used to represent complete switched models of a wide class of power converters, with EDs having characteristics represented by piecewise-affine (even complicated) relations. The model equations can be written in an easy and compact way without the enumeration of all converter modes, eventually formalizing the procedure to an algorithm. The complementarity model can be used to perform transient simulations and time-domain analysis. Mathematical tools coming from nonlinear programming allow to simulate numerically the transient behavior of even complex power converters. Also rigorous time-domain analysis is possible without excluding pathological situations like, for instance, inconsistent initial conditions and simultaneous switchings. Basic converters topologies are used as examples to show the construction procedure for the complementarity models and their usefulness for simulating the dynamic evolution also for non trivial operating conditions.

I. INTRODUCTION

Most power converters can be assumed to consist of linear elements (resistors, inductors, capacitors), voltage and current sources, and electronic devices (EDs) such as diodes and electronic switches (thyristors, transistors, MOSFETs, etc.). A typical way for modeling power converters consists of assuming diodes and switches to be ‘ideal’, discriminating among the different modes of the converter, building for each mode a linear time-invariant dynamic model and determining the conditions for the commutations among the different modes [1], [2]. The resulting model is usually called a *switched* model, which is the model structure used by several power converters simulators such as PLECS™ by PLEXIM and SymPowerSystems™ by TheMathworks. Unfortunately, the commutation conditions can depend on the state variables, e.g. the so-called internally controlled commutations, and the switched model eventually becomes rather complex also for

simple converter topologies [3], [4]. In general a switched model that describes all possible operating conditions, in the sequel indicated as a *complete* switched model, is very difficult to be constructed for converters with more than two EDs. However, by fixing the sequence of modes that alternate due to the commutations of diodes and ideal switches, simplified switched models and the corresponding averaged models, pulse-width-modulation switch models and discrete-time maps can be directly obtained [2], [5]–[9].

In this paper switched complementarity formalism is proposed as a new perspective for obtaining complete switched models of power electronics converters and for simulating their behavior. Complementarity models have been proposed as a framework for modeling (static) resistors–diodes–sources (RDS) circuits, which include only linear resistors, independent voltage and current sources and ideal diodes (IDs) [10], [11]. More recently, switched complementarity systems have been used to model (dynamic) switched electrical networks that contain IDs and ideal switches (ISs) [4], [12], [13]. A preliminary contribution on complementarity models for power converters was presented in [14]. The main idea for the construction of a power converter complementarity model consists of modeling the EDs characteristics separately from the circuit in which they are used and then by integrating the EDs representations with the dynamic equations of the circuit. A similar approach is used for the Modified Nodal Analysis, which is the modeling method chosen for the SPICE-like simulators, such as PSpice [15], where EDs characteristics are represented in details by means of nonlinear smooth algebraic relations. Instead, in this paper, dealing with switched models, the EDs are assumed to be ideal in the sense that their characteristics are represented by possible switching piecewise-affine relations, which is a classical assumption used for modeling and simulation convenience [15]–[18]. In particular, in our approach the power converter is represented as the feedback interconnection of a linear time-invariant dynamic system Σ_d representing the circuit topology, with a set of piecewise-affine characteristics (φ, λ) representing the current–voltage

characteristics of the EDs (see Fig. 1). A minimal state space representation of Σ_d can be obtained by using classical circuit theory methods, given the power converter [19]. The nondecreasing piecewise-affine EDs characteristics are represented in the complementarity form by using RDS equivalent circuits [20], [21]. The interesting feature of the proposed representation is that, if Σ_d is passive, the representation preserves the passivity of the closed loop system which is a property that can be exploited for obtaining well-posedness and stability results [22], [23]. The complementarity model is simple to be built, captures all modes of the converter and allows the idealization of the EDs characteristics at the desired level of abstraction. In order to obtain an efficient time-stepping simulation [24], [25], the proposed models can be numerically integrated by exploiting already available algorithms for the integration of switched complementarity models [26]. Time-domain analysis is possible even for complex power converters and without excluding inconsistent initial conditions and simultaneous switchings, situations that are difficult to be managed with most of the existing simulation tools based on switched models [27].

The paper is organized as follows. In Section II a preliminary example for the illustration of the complementarity modeling procedure is presented. In Section III it is shown how given a piecewise-affine current-voltage characteristic of an ED it can be constructed an equivalent RDS circuit and from that a corresponding (static) complementarity representation. The procedure is generalized for externally controlled EDs in Section IV. In Section V it is shown how to integrate the ED characteristics with the dynamic part of the converter in order to obtain the switched complementarity model of the power converter. The effectiveness of the proposed approach for modeling and simulating power converters is demonstrated in Section VI by considering a dc/dc boost converter and a three phase inverter. By using PSpice as a reference for validation of the results, it is also shown how the proposed approach has some advantages compared to well known simulation softwares based on switched models like PLECS. Section VII points out some conclusions and directions for future research.

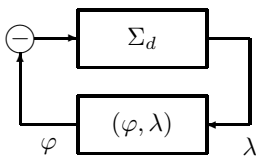


Fig. 1. The feedback representation of the complementarity model of a power converter: Σ_d represents the dynamic part of the circuit and (φ, λ) the set of characteristics of the EDs. The motivation for using a *negative* feedback loop will be clarified in the sequel of the paper.

II. AN ILLUSTRATIVE EXAMPLE

In order to show a preliminary comparison between the classical and the complementarity switched modeling approaches, consider the dc/dc boost converter depicted in Fig. 2. Assume that ED₁ is an ideal diode, i.e. $i_1 \geq 0$ and $v_1 = 0$ if the ID

is conducting and $i_1 = 0$ and $v_1 \geq 0$ if the ID is blocking. (Note that the sign of the ID electrical variables is chosen so that they take nonnegative values.) The electronic device ED₂ is assumed to be the antiparallel connection of an electronic switch and an ID, i.e. $v_2 = 0$ and $i_2 \in \mathbb{R}$ if ED₂ is ON (ED₂ is bidirectional when ON), and (i_2, v_2) corresponding to an ID characteristic if ED₂ is OFF. A typical way of

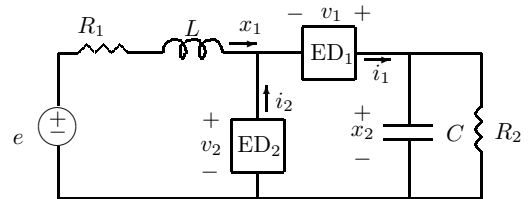


Fig. 2. Circuit scheme of a dc/dc boost converter.

modeling the converter consists of detailing all converter modes corresponding to different states of the switches. When ED₂ is ON then ED₁ is blocking (in usual operating conditions $x_2 > 0$ and thus when ED₂ is ON $v_1 = x_2 > 0$) and one can write $L\dot{x}_1 = -R_1x_1 + e$. When ED₂ is turned OFF, for positive inductor current the diode ED₁ will be conducting and it follows $L\dot{x}_1 = -R_1x_1 - x_2 + e$. If the inductor current x_1 goes to zero the converter will start operating in discontinuous conduction mode and the current will remain identically zero until ED₂ is turned ON again. The dynamics of the capacitor voltage can be expressed as $C\dot{x}_2 = -x_2/R_2$ when ED₁ is blocking and as $C\dot{x}_2 = x_1 - x_2/R_2$ when ED₁ is conducting. The described behavior can be simply formalized by means of a switched model. In spite of the simplicity of the behavior, also for this quite simple converter topology several subtleties are hidden under the descriptive features of the converter model. Indeed the description does not capture (or excludes) several scenarios, e.g. inconsistent initial conditions corresponding to a negative capacitor voltage. Furthermore, in describing the behavior, some implicit reasonings have been done: for example when the converter goes into discontinuous conduction mode a negative inductor current is excluded although in principle it could flow through the antiparallel diode of ED₂. Only by considering the whole dynamics, together with constraints given by the variables of the switches, it becomes evident that such situation has to be excluded. In general, a complete switched model becomes rather complex to be obtained also for simple converter topologies, and the problem becomes more and more difficult when the number of EDs increases.

Switched complementarity models are an interesting alternative to classical approaches for determining a complete switched model of a power converter. Consider again the converter in Fig. 2. By applying the Kirchhoff laws it follows:

$$L\dot{x}_1 = -R_1x_1 - x_2 + v_1 + e \quad (1a)$$

$$C\dot{x}_2 = x_1 - \frac{1}{R_2}x_2 + i_2 \quad (1b)$$

$$i_1 = x_1 + i_2 \quad (1c)$$

$$v_2 = x_2 - v_1 \quad (1d)$$

which must be satisfied independently of the commutations of the EDs. In order to obtain a complete model, the equations (1) must be integrated with the EDs characteristics (i_1, v_1) and (i_2, v_2) . The ideal EDs characteristics can be analytically represented as

$$0 \leq v_1 \perp i_1 \geq 0 \quad (2a)$$

$$\mathbb{R} \ni i_2 \perp v_2 = 0, \quad \text{when switch ED}_2 \text{ is ON} \quad (2b)$$

$$0 \leq i_2 \perp v_2 \geq 0, \quad \text{when switch ED}_2 \text{ is OFF}, \quad (2c)$$

where \perp is the orthogonality symbol, i.e. given two real vectors z and w the notation $z \perp w$ stands for $z^T w = 0$ (the scalar product is zero), for notation simplicity ' $\mathbb{R} \ni i$ ' is sometimes used standing for ' $i \in \mathbb{R}$ ', and ' $i \in \mathbb{R}_+$ ' or ' $i \geq 0$ ' are equivalently used throughout the paper. Note that conditions (2) imply that for each pair (i_1, v_1) and (i_2, v_2) one of the two electrical variables must be zero. The model (1)-(2) can be rewritten in the so-called switched cone complementarity form

$$\dot{x} = Ax + Bz + Eu + g \quad (3a)$$

$$w = Cx + Dz + Fu + h \quad (3b)$$

$$\mathcal{C}_\pi^* \ni z \perp w \in \mathcal{C}_\pi \quad (3c)$$

where x is the state vector, u is the vector of external inputs, A, B, C, D, E, F, g and h are constant matrices, (z, w) are the so-called complementarity variables [28]. In particular, for the dc/dc boost converter $x = [x_1 \ x_2]^T$, $u = e$, $z = [v_1 \ i_2]^T$ and $w = [i_1 \ v_2]^T$. The sets \mathcal{C}_π^* and \mathcal{C}_π depend on the externally controlled commutations: if ED₂ is ON from (2a)-(2b) it follows that $\mathcal{C}_\pi^* = \mathbb{R}_+ \times \mathbb{R}$ and $\mathcal{C}_\pi = \mathbb{R}_+ \times \{0\}$, whereas if ED₂ is OFF from (2a) and (2c) it follows $\mathcal{C}_\pi^* = \mathcal{C}_\pi = \mathbb{R}_+ \times \mathbb{R}_+$. With the above positions (3) becomes a complete switched model of the dc/dc boost converter. The model (3) captures the converter behavior in all possible operating conditions. For instance, assume that ED₂ is OFF and that at a time instant say \bar{t} the inductor current becomes zero. As it is well known such condition determines the converter to operate in discontinuous conduction mode. It is easy to show that having $x_1(t) < 0$ for $t \in (\bar{t}, \bar{t} + \epsilon_1]$ and any $\epsilon_1 > 0$ is not possible for a solution of the complementarity model (1)-(2) because some of the constraints (2) are violated. Indeed, since $x_1(\bar{t}) = 0$, in order to get a negative current one should have $\dot{x}_1(t) < 0$ for $t \in (\bar{t}, \bar{t} + \epsilon_2]$ with some $\epsilon_2 > 0$. From (1a) and (1d) it follows $v_2 = -L\dot{x}_1 - R_1x_1 + e$ and if $\dot{x}_1 < 0$ it is v_2 strictly positive and from (2c) $i_2 = 0$. Then from (1c) one has $i_1 = x_1$ and the constraint (2a) contradicts the hypothesis of having a negative current. Similar considerations can be done for the other converter modes and for detecting inconsistent initial conditions.

In the sequel we show that complete switched models of a wide class of power converters can be represented in the form (3). Note that in (3a)-(3b) all matrices are constant, the internally controlled commutations are taken into account by means of nonnegative inequality constraints in (3c), and the externally controlled commutations determine a change in the sets \mathcal{C}_π^* and \mathcal{C}_π . When an ED is neither an ID nor an IS, its current-voltage characteristic can be represented by means of a more generic piecewise-affine relation. In that case, in order to obtain a complementarity model (3) some intermediate steps must be carried out. In particular, voltage and current of the ED will not correspond to complementarity variables. On the other hand, a different idealization of the EDs characteristics should not affect the equations that describe the circuit topology, e.g. (1). The EDs variables that appear into the dynamic equations, e.g. v_1 and i_2 in (1a) and (1b), will be considered as 'inputs' for the circuit model part and indicated by using the symbol φ with suitable subscripts, see the block Σ_d in Fig. 1. The other EDs variables, e.g. i_1 and v_2 , will be considered as 'outputs' for the circuit model part Σ_d and denoted by λ . The representation of the (φ, λ) ED characteristic will bring into the model the complementarity variables z and w , and will allow to write the model in the form (3). As a preliminary step towards the determination of the switched cone complementarity model (3), in next section we show how it is possible to obtain a complementarity representation of a piecewise-affine (φ, λ) characteristic by using equivalent RDS circuit representations.

III. COMPLEMENTARITY MODEL OF PIECEWISE-AFFINE CHARACTERISTICS VIA RDS CIRCUITS

Throughout the paper we deal with EDs whose current-voltage characteristics can be idealized by means of scalar piecewise-affine nondecreasing characteristics. To elaborate on this, let (φ, λ) be a pair of current and voltage, or vice versa. Let us introduce first some useful definitions. The (φ, λ) characteristic changes its slope at the so-called *breaking points*. Then the idealized ED characteristic is uniquely defined by the initial slope σ_0 , the final slope σ_p and the set of p breaking points $\{(\Phi_j, \Lambda_j), j = 1, \dots, p\}$ with the intermediate slopes $\sigma_j, j = 1, \dots, p-1$. The slope of the j th affine part of the characteristic will be

$$\sigma_j \triangleq \frac{\Phi_{j+1} - \Phi_j}{\Lambda_{j+1} - \Lambda_j}, \quad j = 1, \dots, p-1. \quad (4)$$

Since we deal only with nondecreasing characteristics we have $\sigma_j \geq 0$ for $j = 0, 1, \dots, p$. The slope can assume infinity as a value. Moreover, from the definition of breaking point it follows $\sigma_j \neq \sigma_{j-1}$ for $j = 1, \dots, p$. The j th breaking point is called a *convex breaking point* if $\sigma_j > \sigma_{j-1}$ and a *concave breaking point* if $\sigma_j < \sigma_{j-1}$. In what follows we show that any nondecreasing piecewise-affine relation between φ and λ can be represented by an equivalent RDS circuit and then parameterized by the complementarity variables z and w in

the following complementarity form:

$$\varphi = a_s \lambda + b_s^T z + g_s \quad (5a)$$

$$w = c_s \lambda + D_s z + h_s \quad (5b)$$

$$0 \leq z \perp w \geq 0, \quad (5c)$$

where $a_s \geq 0$, $b_s \in \mathbb{R}^p$, $g_s \in \mathbb{R}$, $c_s \in \mathbb{R}^p$, $D_s \in \mathbb{R}^{p \times p}$, $h_s \in \mathbb{R}^p$. The relation (5c) implies that for each pair of complementarity variables at least one of them must be zero. Each pair of complementarity variables (z_j, w_j) will represent current and voltage of an ID appearing in the RDS circuit. In our complementarity representation the number of complementarity variables, i.e. the length of the vectors z and w , is equal to the number of breaking points of the characteristic. As it will be shown in the sequel different RDS circuits can equivalently represent the same (φ, λ) characteristic.

A. Nondecreasing single breaking point characteristics

The complementarity model (5) for the characteristic of the so-called ideal diode (ID), see Fig. 3, can be simply obtained. Indeed, such a (φ, λ) characteristic can be written in the complementarity form (5) with $\varphi = z$ and $w = -\lambda$, i.e. $a_s = 0$, $b_s = 1$, $g_s = 0$, $c_s = -1$, $D_s = 0$, $h_s = 0$ and $0 \leq z \perp w \geq 0$. The ID characteristic is a

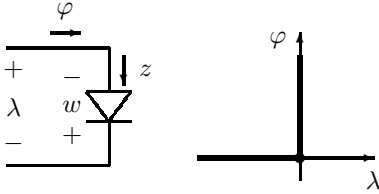


Fig. 3. Ideal diode symbol with the corresponding (φ, λ) current-voltage characteristic and the indication of a possible pair of complementarity variables.

particular case of a piecewise-affine nondecreasing convex characteristic, compare Fig. 3 and Fig. 4. By using the ID behavior it is possible to show that the (φ, λ) characteristic depicted in Fig. 4 represents the current-voltage characteristic for the circuit shown in the same figure. Note that in [21] the series of a resistor, an ID and a voltage source is called a *concave resistor*. The (φ, λ) characteristic in Fig. 4 can be represented by integrating both blocking and conducting states of the ID into the following complementarity model:

$$\varphi = g_0 \lambda + z_1 + \Phi_0 \quad (6a)$$

$$w_1 = -\lambda + \frac{1}{g_1} z_1 + \Lambda_1 \quad (6b)$$

$$0 \leq z_1 \perp w_1 \geq 0. \quad (6c)$$

The model (6) can be explained by analyzing conducting and blocking operating conditions of the ID. Since $z_1 \geq 0$, from (6b) it follows that for $\lambda < \Lambda_1$ it will be $w_1 > 0$. Then it must be $z_1 = 0$ and the ID is blocking. Equation (6a) becomes $\varphi = g_0 \lambda + \Phi_0$, which by choosing $g_0 \triangleq \sigma_0 \geq 0$ is the equation of the initial affine part of the characteristic. For $\lambda > \Lambda_1$, since w_1 must be nonnegative, from (6b) it follows that z_1 must be strictly positive and then the ID will be conducting,

i.e. $w_1 = 0$. By substituting z_1 obtained from (6b) in (6a) we get $\varphi = (g_0 + g_1)\lambda - g_1 \Lambda_1 + \Phi_0$. Then by choosing $g_1 \triangleq \sigma_1 - \sigma_0 > 0$ we get $\varphi = \sigma_1 \lambda - (\sigma_1 - \sigma_0)\Lambda_1 + \Phi_0$ which is the equation of the affine part of the characteristic in Fig. 4 with slope σ_1 . It can be shown that (6) is a complementarity representation of any piecewise-affine nondecreasing and convex (φ, λ) characteristic with only one breaking point, independently of what type of variables (current or voltage) φ and λ are [29]. Therefore below, without loss of generality, we assume that φ is a current and λ is a voltage, so as in Fig. 4.

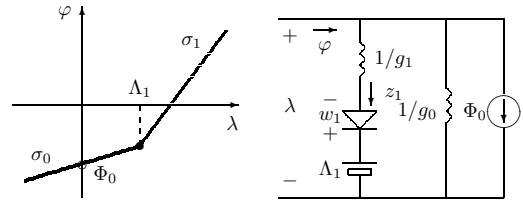


Fig. 4. Piecewise-affine nondecreasing convex characteristic (φ, λ) with a single breaking point and a corresponding RDS circuit; here $1/g_0$ and $1/g_1$ are resistances; Φ_0 is the intersection of the initial affine part of the characteristic with the φ -axis. The ID characteristic in Fig. 3 can be obtained as a particular case with $\Phi_0 = 0$, $\Lambda_1 = 0$, $\sigma_0 = g_0 = 0$ and $\sigma_1 = g_1$ infinite.

Consider the piecewise-affine nondecreasing concave single breaking point characteristic in Fig. 5. By using the ID behavior and arguments similar to those presented above, it is simple to show that the (φ, λ) characteristic represents the current-voltage characteristic for the circuit depicted in the same figure. Note that in [21] the parallel of a resistor, an ID and a current source is called a *convex resistor*. By applying the KCL and KVL to the circuit the (φ, λ) characteristic can be represented in the following complementarity form:

$$\varphi = \frac{1}{r_0 + r_1} (\lambda - r_1 z_1 - \Lambda_0 + r_1 \Phi_1) \quad (7a)$$

$$w_1 = \frac{r_1}{r_0 + r_1} (\lambda + r_0 z_1 - \Lambda_0 - r_0 \Phi_1) \quad (7b)$$

$$0 \leq z_1 \perp w_1 \geq 0, \quad (7c)$$

where $r_0 \triangleq \frac{1}{\sigma_0} \geq 0$ and $r_1 \triangleq \frac{1}{\sigma_1} - \frac{1}{\sigma_0} > 0$. By imposing $r_0 = 0$, $\Phi_1 = 0$, $\Lambda_0 = 0$ and letting $r_1 \rightarrow +\infty$, the model (7) becomes the complementarity representation of an ID in which $\varphi = -z_1$ is the opposite of the nonnegative ID current and $\lambda = w_1$ is the nonnegative ID voltage.

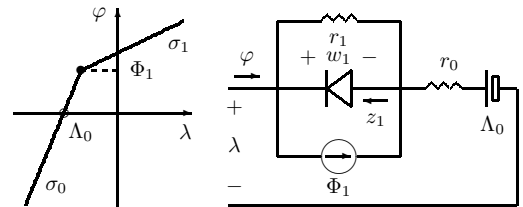


Fig. 5. Piecewise-affine nondecreasing concave characteristic (φ, λ) with a single breaking point and a corresponding RDS circuit; here r_0 and r_1 are resistances; Λ_0 is the intersection of the initial affine part of the characteristic with the λ -axis.

B. Nondecreasing convex characteristics

Consider the piecewise-affine nondecreasing convex characteristic in Fig. 6. All breaking points are convex and $\sigma_j > \sigma_{j-1} \geq 0$ for $j = 1, \dots, p$. Fig. 6 represents the current-voltage characteristic of the RDS circuit in Fig. 7, where $p = 3$ and

$$g_0 \triangleq \sigma_0 \quad (8a)$$

$$g_j \triangleq \sigma_j - \sigma_{j-1}, \quad j = 1, \dots, p. \quad (8b)$$

Note that $g_0 \geq 0$ and $g_j > 0$ for $j = 1, \dots, p$, i.e. all resistances in Fig. 7 are positive. The circuit topology can be explained by noticing that the RDS circuit in Fig. 7 is obtained from that in Fig. 4 by adding concave resistors in parallel, one for each breaking point. For $\lambda < \Lambda_1$ all IDs are blocking; for $\Lambda_1 < \lambda < \Lambda_2$ the first ID is conducting and all the other IDs are blocking; for $\Lambda_2 < \lambda < \Lambda_3$ the first two IDs are conducting; and so on. In other words the j th ID will be conducting if $\lambda > \Lambda_j$. Note that if the characteristic has a final vertical piece, one has $1/g_p = 0$ and a shortcut will replace the resistance in the p th concave resistor of the RDS circuit in Fig. 7. By applying the KCL and KVL to the RDS

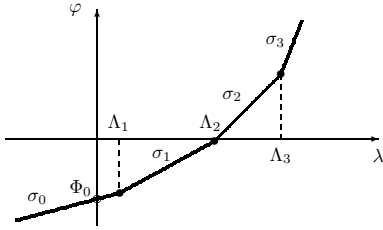


Fig. 6. Piecewise-affine nondecreasing convex (φ, λ) characteristic with $p = 3$ breaking points.

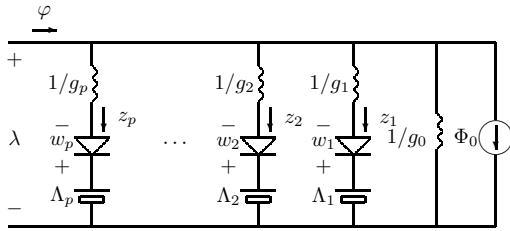


Fig. 7. A RDS circuit that has a piecewise-affine convex current-voltage (φ, λ) characteristic. A pair of complementarity variables is associated to each ID; $1/g_j$, $j = 0, \dots, p$ are resistances.

circuit in Fig. 7 we get:

$$\varphi = g_0 \lambda + \sum_{k=1}^p z_k + \Phi_0 \quad (9a)$$

$$w_j = -\lambda + \frac{1}{g_j} z_j + \Lambda_j, \quad j = 1, \dots, p. \quad (9b)$$

Moreover the IDs characteristics can be modeled as:

$$0 \leq z_j \perp w_j \geq 0, \quad j = 1, \dots, p. \quad (10)$$

The complementarity representation (9)-(10) of a piecewise-affine nondecreasing convex (φ, λ) characteristic can be simply rewritten in the form (5).

C. Nondecreasing concave characteristics

Consider the nondecreasing concave (φ, λ) characteristic shown in Fig. 8. All breaking points are concave then $0 \leq \sigma_j < \sigma_{j-1}$ for $j = 1, \dots, p$. The characteristic in Fig. 8 represents the current-voltage characteristic of the RDS circuit in Fig. 9, where $p = 3$ and

$$r_0 \triangleq \frac{1}{\sigma_0} \quad (11a)$$

$$r_j \triangleq \frac{1}{\sigma_j} - \frac{1}{\sigma_{j-1}}, \quad j = 1, \dots, p. \quad (11b)$$

The RDS circuit is obtained from that in Fig. 5 by adding convex resistors in series. For $\varphi < \Phi_1$ all IDs are conducting, for $\Phi_1 < \varphi < \Phi_2$ only the first ID is blocking, and so on. In other words, the j th ID will be blocking if $\varphi > \Phi_j$. If the characteristic has a final horizontal part, one has $\sigma_p = 0$ and consequently r_p is replaced by an open circuit. Note that in this case if $p > 1$, the ID in the p th convex resistor requires a different choice of the complementarity variables in order to get a complementarity representation (see (13b) below).

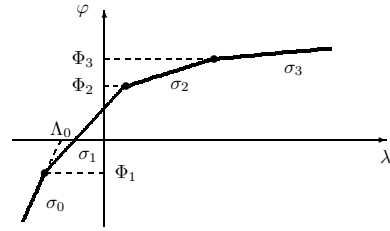


Fig. 8. Piecewise-affine nondecreasing concave (φ, λ) characteristic with $p = 3$ breaking points; Λ_0 is the intersection of the (continuation of the) initial affine part (the one with slope σ_0) with the λ -axis.

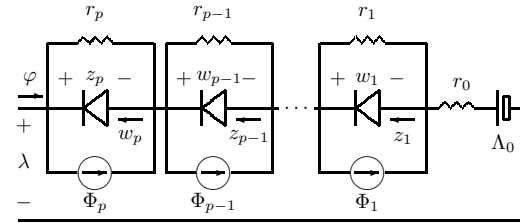


Fig. 9. A RDS circuit that has a nondecreasing concave current-voltage (φ, λ) characteristic.

Indeed by applying the KVL to the RDS circuit in Fig. 7 we get:

$$\lambda = r_0 \varphi + \sum_{k=1}^{p-1} w_k + z_p + \Lambda_0. \quad (12)$$

By applying the KCL at the different nodes of the circuit in Fig. 7 we get:

$$w_j = r_j \varphi + r_j z_j - r_j \Phi_j, \quad j = 1, \dots, p-1 \quad (13a)$$

$$w_p = -\varphi + \frac{z_p}{r_p} + \Phi_p. \quad (13b)$$

By substituting (13a) in (12) and solving for φ :

$$\varphi = \frac{1}{\sum_{k=0}^{p-1} r_k} \lambda - \frac{\sum_{k=1}^{p-1} r_k z_k + z_p}{\sum_{k=0}^{p-1} r_k} + \frac{\sum_{k=1}^{p-1} r_k \Phi_k - \Lambda_0}{\sum_{k=0}^{p-1} r_k}. \quad (14)$$

Note that $\sum_{k=0}^{p-1} r_k = 1/\sigma_{p-1}$. Then (14) is well posed provided that σ_{p-1} is finite. The condition σ_{p-1} being infinite corresponds to a nondecreasing concave characteristic with one breaking point and infinite slope of the initial part, i.e. $p = 1$ and σ_0 infinite. Such situation is already included in the model (7) with $r_0 = 0$. By substituting (14) in (13) we get the complementarity model (5).

D. Nondecreasing characteristics

It is possible to construct now a complementarity model for a generic piecewise-affine nondecreasing (φ, λ) characteristic, defined by the set of breaking points, the initial slope and the final slope. The breaking points set can be divided into the sequences of consecutive convex and concave breaking points. A sequence of consecutive convex (concave) breaking points is also called a *convex (concave) sequence*. By using a procedure similar to that presented above, to each convex (concave) sequence one can associate an equivalent RDS circuit. Then an RDS circuit having (φ, λ) as current-voltage characteristic can be obtained by collecting and by connecting the RDS circuits corresponding to the different breaking points sequences. By using such circuit it is possible to formulate an algorithm for the construction of a complementarity model of any piecewise-affine nondecreasing characteristic, see [29] for the details.

As example consider the piecewise-affine representation of a diode characteristic shown in Fig. 10. The (φ, λ) characteristic has two breaking points: $(0, V_B)$ is concave and $(0, V_F)$ is convex. The characteristic corresponds to the current-voltage characteristic of the RDS circuit depicted in Fig. 11. The circuit is obtained by connecting the RDS circuit corresponding to the concave breaking point $(0, V_B)$ (Fig. 5 with $\Lambda_0 = V_B$, $r_0 = 0$, r_1 replaced by an open circuit and $\Phi_1 = 0$) with the RDS circuit corresponding to the convex breaking point $(0, V_F)$ (Fig. 4 with $\Phi_0 = 0$, $g_0 = 0$, $1/g_1 = R_{ON}$ and $\Lambda_1 = V_F$). By applying the KVL and KCL to the circuit in Fig. 11 one can write

$$\varphi_1 = -z_1 \quad (15a)$$

$$\varphi_2 = z_2 \quad (15b)$$

$$w_1 = \lambda_1 - V_B \quad (15c)$$

$$w_2 = -\lambda_2 + R_{ON} z_2 + V_F \quad (15d)$$

$$\varphi = \varphi_1 + \varphi_2 \quad (15e)$$

$$\lambda = \lambda_1 = \lambda_2. \quad (15f)$$

By substituting λ for λ_1 and λ_2 in (15c) and (15d), and by using (15e) the complementarity model of the (φ, λ) characteristic in Fig. 10 can be represented in the form (5) with the following matrices:

$$a_s = 0, \quad b_s^T = [-1 \quad 1], \quad g_s = 0, \quad (16a)$$

$$c_s = \begin{bmatrix} 1 \\ -1 \end{bmatrix}, \quad D_s = \begin{bmatrix} 0 & 0 \\ 0 & R_{ON} \end{bmatrix}, \quad h_s = \begin{bmatrix} -V_B \\ V_F \end{bmatrix}. \quad (16b)$$

Note that two pairs of complementarity variables are needed

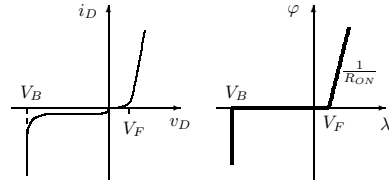


Fig. 10. Current-voltage characteristic of a diode and a corresponding idealized piecewise-affine characteristic: V_B is the breakdown voltage and V_F is the forward voltage.

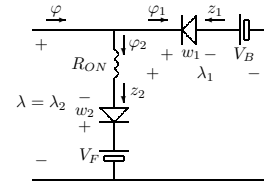


Fig. 11. RDS circuit corresponding to the piecewise-affine diode characteristic in Fig. 10.

in order to represent the piecewise-affine diode characteristic in Fig. 10 whereas only one pair of complementarity variables is enough for the ID. The motivation for that is on the number of breaking points of the two characteristics. In general different complementarity representations can be obtained with a different choice of the z and w variables.

IV. CONE COMPLEMENTARITY MODELS FOR SWITCHING ELECTRONIC DEVICES

In the analysis above we have considered only uncontrolled EDs. In order to represent the characteristics of switching EDs, i.e. EDs whose state can be forced ON and OFF, we need to generalize the model (5) in the so-called *cone complementarity form*. Introduce first the complementarity model of the ideal switch (IS). Without loss of generality, let z_{IS} be the voltage across the switch and w_{IS} the current through the switch. The behavior of an IS can be represented with $z_{IS} = 0$ and $w_{IS} \in \mathbb{R}$ if the IS is ON, and $z_{IS} \in \mathbb{R}$ and $w_{IS} = 0$ if the IS is OFF, see Fig. 12. Such relations can be rewritten in the following form

$$\mathcal{K}_\pi^* \ni z_{IS} \perp w_{IS} \in \mathcal{K}_\pi \quad (17)$$

where $\pi = 1$ if IS is ON, $\pi = -1$ if IS is OFF, and we define the following sets

$$\mathcal{K}_0 = \mathcal{K}_0^* = \mathbb{R}_+, \quad (18a)$$

$$\mathcal{K}_1 = \mathbb{R}, \quad \mathcal{K}_1^* = \{0\}, \quad (18b)$$

$$\mathcal{K}_{-1} = \{0\}, \quad \mathcal{K}_{-1}^* = \mathbb{R}, \quad (18c)$$

The sets \mathcal{K}_0 , \mathcal{K}_1 and \mathcal{K}_{-1} are cones and the sets \mathcal{K}_0^* , \mathcal{K}_1^* and \mathcal{K}_{-1}^* are the corresponding dual cones [12]. The novelty of (17) with respect to the complementarity condition (5c) is that the IS model can also represent the commutations by means of the switching function π which can be time-varying. Moreover the model (17) includes also the representation of an ID, which can be obtained by choosing a constant $\pi = 0$.

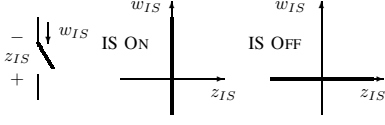


Fig. 12. Ideal switch with the complementarity variables and the corresponding characteristics in ON and OFF states. Note that, so as for the ID, the complementarity variables z_{IS} and w_{IS} are chosen with the source sign convention.

By using the IS device it is possible to model in the cone complementarity framework any ED whose current–voltage characteristics in the ON and OFF states are representable in a piecewise–affine form. Say $(\varphi_{ON}, \lambda_{ON})$ the characteristic of the ED when ON and $(\varphi_{OFF}, \lambda_{OFF})$ when OFF. Consider the circuit in Fig. 13 where φ is the current and λ is the voltage of the ED to be modeled. Two ISs are used and their states are controlled so that for each state of the ED only one leg of the parallel determines the ED behavior. When the ED is ON, one has to assign IS₁ ON ($\pi_1 = 1$) and IS₂ OFF ($\pi_2 = -1$), so that the characteristic (φ, λ) is represented by the equivalent impedance ξ_{ON} , i.e. $\varphi = \varphi_{ON}$ and $\lambda = \lambda_{ON}$. Vice versa if the ED is OFF one fixes IS₁ OFF ($\pi_1 = -1$) and IS₂ ON ($\pi_2 = 1$), so that $\varphi = \varphi_{OFF}$, $\lambda = \lambda_{OFF}$ and the characteristic of the ED is represented by the equivalent impedance ξ_{OFF} . Then for any state of the ED we can write

$$\varphi = w_{IS_1} + w_{IS_2} \quad (19a)$$

$$\begin{aligned} w_{IS_1} &= \varphi_{ON} = a_{ON}\lambda_{ON} + b_{ON}^T z_{ON} + g_{ON} \\ &= a_{ON}\lambda + a_{ON}z_{IS_1} + b_{ON}^T z_{ON} + g_{ON} \end{aligned} \quad (19b)$$

$$w_{IS_2} = \varphi_{OFF} = a_{OFF}\lambda + a_{OFF}z_{IS_2} + b_{OFF}^T z_{OFF} + g_{OFF} \quad (19c)$$

$$w_{ON} = c_{ON}\lambda + c_{ON}z_{IS_1} + D_{ON}z_{ON} + h_{ON} \quad (19d)$$

$$w_{OFF} = c_{OFF}\lambda + c_{OFF}z_{IS_2} + D_{OFF}z_{OFF} + h_{OFF}. \quad (19e)$$

Equations (19) can be rewritten in the form

$$\varphi = a_s \lambda + b_s^T z + g_s \quad (20a)$$

$$w = c_s \lambda + D_s z + h_s \quad (20b)$$

$$\mathcal{C}_\pi^* \ni z \perp w \in \mathcal{C}_\pi, \quad (20c)$$

where

$$z^T = [z_{IS_1} \quad z_{IS_2} \quad z_{ON} \quad z_{OFF}] \quad (21a)$$

$$w^T = [w_{IS_1} \quad w_{IS_2} \quad w_{ON} \quad w_{OFF}] \quad (21b)$$

$$a_s = a_{ON} + a_{OFF}, \quad b_s^T = [a_{ON} \quad a_{OFF} \quad b_{ON}^T \quad b_{OFF}^T], \quad (21c)$$

$$g_s = g_{ON} + g_{OFF}, \quad (21d)$$

$$c_s = \begin{bmatrix} a_{ON} \\ a_{OFF} \\ c_{ON} \\ c_{OFF} \end{bmatrix}, \quad h_s = \begin{bmatrix} g_{ON} \\ g_{OFF} \\ h_{ON} \\ h_{OFF} \end{bmatrix}, \quad (21e)$$

$$D_s = \begin{bmatrix} a_{ON} & 0 & b_{ON}^T & 0 \\ 0 & a_{OFF} & 0 & b_{OFF}^T \\ c_{ON} & 0 & D_{ON} & 0 \\ 0 & c_{OFF} & 0 & D_{OFF} \end{bmatrix}, \quad (21f)$$

$$\mathcal{C}_\pi = \mathcal{K}_{\pi_1} \times \mathcal{K}_{\pi_1}^* \times \mathbb{R}_+^{p_{ON}} \times \mathbb{R}_+^{p_{OFF}}, \quad (21g)$$

$$\mathcal{C}_\pi^* = \mathcal{K}_{\pi_1}^* \times \mathcal{K}_{\pi_1} \times \mathbb{R}_+^{p_{ON}} \times \mathbb{R}_+^{p_{OFF}} \quad (21h)$$

with $\pi_1 = 1$ ($\pi_2 = -1$) if the ED is ON and $\pi_1 = -1$ ($\pi_2 = 1$) if the ED is OFF, p_{ON} and p_{OFF} being the numbers of breaking points (and IDs) for the $(\varphi_{ON}, \lambda_{ON})$ and $(\varphi_{OFF}, \lambda_{OFF})$ characteristics, respectively. The representations of both states of the ED (ON and OFF) are now included in (20).

If the ED behaves as a shortcut when ON (as an open circuit when OFF, respectively) the circuit in Fig. 13 can be simplified to the parallel (series) connection of an IS with the equivalent impedance of the OFF (ON) phase. If φ is a voltage and λ is a current one can obtain the cone complementarity representation by using dual circuits [29]. It should be noticed

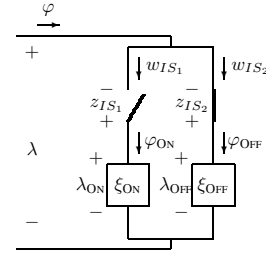


Fig. 13. Circuit for the complementarity representation of the current–voltage characteristics of a switching ED. The RDS circuits corresponding to the characteristics in the ON and OFF states are represented by the equivalent impedances ξ_{ON} and ξ_{OFF} , respectively.

that by exploiting the specific ED characteristic it is possible to obtain representations that involve a lower number of complementarity variables. Moreover there exist some changes of the characteristics of ξ_{ON} and ξ_{OFF} that affect only the vectors g_s and h_s in the representation (20). In particular this is the case for variations of the characteristic such that the number of breaking points and the slopes of each sequence of breaking points do not change. That could be useful to prove robust stability under specific uncertainties of the characteristics.

V. COMPLEMENTARITY MODELS FOR POWER CONVERTERS

In the previous analysis we have shown that any switching piecewise–affine characteristic of an ED can be represented in the cone complementarity form (20) where (φ, λ) is the pair of current and voltage (or vice versa) of the device and (z, w) is the pair of vectors of the complementarity variables associated to that device. In the first part of this section we show how, given the representations of the EDs of a power converter, it is possible to obtain the representation of the entire converter. In the second part of the section a possible approach for the numerical integration of the model is presented.

A. Switched cone complementarity model

Consider current and voltage on each i th ED as an input φ_{d_i} or as an output λ_{d_i} for the remaining part of the circuit which represents the dynamic part of the system. We assume for the sign of voltage and current on the EDs the convention used for sources. Such choice is important to check passivity of the dynamic model of the converter with respect to the input φ_d and the output λ_d [23]. On the other hand, since the typical voltage and current sign convention chosen for the ED characteristic representation is the opposite, i.e. the one used

for passive components, that motivates the negative feedback in Fig. 1 which can be now more specifically represented so as shown in Fig. 14 and with a different representation in Fig. 15. The circuit obtained by extracting N_s EDs, which will consist of linear elements (resistors, inductors and capacitors) and external sources, under very general assumptions [19], can be described by the state-space system

$$\dot{x} = A_d x + B_d \varphi_d + E_d u \quad (22a)$$

$$\lambda_d = C_d x + D_d \varphi_d + F_d u \quad (22b)$$

where x is the state vector, u denotes the external sources, φ_d and λ_d are vectors with N_s components, and $(\varphi_{s_i}, \lambda_{s_i}) = (-\varphi_{d_i}, \lambda_{d_i})$ represents the characteristic of the i th ED. Note that possible state reduction, e.g. a three phase converter with currents equilibrium on the ac side, can be handled at this modeling stage following the typical approach used for classical state space representations of power electronics systems.

Now collect the complementarity models (20) of the N_s EDs of the power converter into the following cone complementarity model:

$$\varphi_s = \tilde{A}_s \lambda_s + \tilde{B}_s z + \tilde{g}_s \quad (23a)$$

$$w = \tilde{C}_s \lambda_s + \tilde{D}_s z + \tilde{h}_s \quad (23b)$$

$$C_\pi^* \ni z \perp w \in C_\pi \quad (23c)$$

$$C_\pi = \prod_{i=1}^{N_s} (\mathcal{K}_{\pi_i} \times \mathcal{K}_{\pi_i}^* \times \mathbb{R}_+^{p_{ON_i}} \times \mathbb{R}_+^{p_{OFF_i}}) \quad (23d)$$

where $\varphi_s \in \mathbb{R}^{N_s}$, $\lambda_s \in \mathbb{R}^{N_s}$, $\tilde{A}_s \in \mathbb{R}^{N_s \times N_s}$, $\tilde{B}_s \in \mathbb{R}^{N_s \times \tilde{p}}$ with $\tilde{p} = \sum_{i=1}^{N_s} (2 + p_{ON_i} + p_{OFF_i})$, $\tilde{g}_s \in \mathbb{R}^{N_s}$, $\tilde{C}_s \in \mathbb{R}^{\tilde{p} \times N_s}$, $\tilde{D}_s \in \mathbb{R}^{\tilde{p} \times \tilde{p}}$, $\tilde{h}_s \in \mathbb{R}^{\tilde{p}}$. The matrices above are given by

$$\tilde{A}_s = \text{diag} \{a_{s_i}\} \geq 0 \quad i = 1, \dots, N_s \quad (24a)$$

$$\tilde{B}_s = \begin{bmatrix} b_{s1}^T & 0 & \dots & 0 \\ 0 & b_{s2}^T & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & b_{sN_s}^T \end{bmatrix} \quad (24b)$$

$$\tilde{g}_s = \text{col} \{g_{s_i}\} \quad i = 1, \dots, N_s \quad (24c)$$

$$\tilde{C}_s = \begin{bmatrix} c_{s1} & 0 & \dots & 0 \\ 0 & c_{s2} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & c_{sN_s} \end{bmatrix} \quad (24d)$$

$$\tilde{D}_s = \text{diag} \{D_{s_i}\} \quad i = 1, \dots, N_s \quad (24e)$$

$$\tilde{h}_s = \text{col} \{h_{s_i}\} \quad i = 1, \dots, N_s \quad (24f)$$

where ‘diag’ indicates block diagonal matrices and ‘col’ indicates matrices obtained by appending in a unique column several scalars or column vectors. By using $\varphi_d = -\varphi_s$ and $\lambda_d = \lambda_s$ (see the feedback scheme in Fig. 14) and by substituting (23a) in (22) one obtains:

$$\dot{x} = A_d x - B_d \left[\tilde{A}_s \lambda_d + \tilde{B}_s z + \tilde{g}_s \right] + E_d u \quad (25a)$$

$$\lambda_d = C_d x - D_d \left[\tilde{A}_s \lambda_d + \tilde{B}_s z + \tilde{g}_s \right] + F_d u \quad (25b)$$

$$w = \tilde{C}_s \lambda_d + \tilde{D}_s z + \tilde{h}_s. \quad (25c)$$

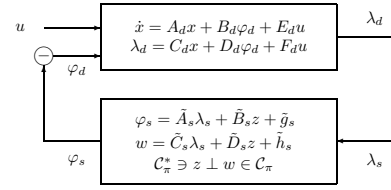


Fig. 14. Feedback structure for the switched cone complementarity model of a power electronic converter.

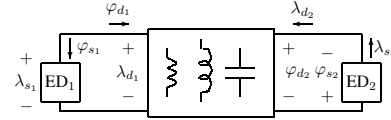


Fig. 15. Block scheme of the power electronic converter with ‘external’ electronic devices. For simplicity external sources are not shown.

By looking at (25b) if the matrix $D_d \tilde{A}_s$ has no eigenvalues in -1 , the matrix $M \triangleq I + D_d \tilde{A}_s \in \mathbb{R}^{N_s \times N_s}$ is invertible and

$$\lambda_d = M^{-1} \left[C_d x - D_d \tilde{B}_s z - D_d \tilde{g}_s + F_d u \right]. \quad (26)$$

Note that being M singular, it means that the feedback structure has an algebraic loop not solvable and we get an ill-posed problem. In the case $D_d > 0$ and $\tilde{A}_s \geq 0$, the matrix $M = (I + D_d \tilde{A}_s)$ is invertible [30]. The same can be proved if $D_d \geq 0$ and $\tilde{A}_s \geq 0$ and diagonal [29], which is the case for the proposed complementarity model ($D_d \geq 0$ follows from passivity of Σ_d and $\tilde{A}_s \geq 0$ from (24a) because the EDs characteristics are assumed to be nondecreasing). By using (26) after some algebra the equations (25a) and (25c) can be written in the switched cone complementarity form (3), which is here repeated for the sake of readability:

$$\dot{x} = A x + B z + E u + g \quad (27a)$$

$$w = C x + D z + F u + h \quad (27b)$$

$$C_\pi^* \ni z \perp w \in C_\pi \quad (27c)$$

with the cones given by (23d) and

$$A := A_d - B_d \tilde{A}_s M^{-1} C_d, \quad (28a)$$

$$B := B_d \tilde{A}_s M^{-1} D_d \tilde{B}_s - B_d \tilde{B}_s, \quad (28b)$$

$$C := \tilde{C}_s M^{-1} C_d, \quad (28c)$$

$$D := \tilde{D}_s - \tilde{C}_s M^{-1} D_d \tilde{B}_s, \quad (28d)$$

$$E := -B_d \tilde{A}_s M^{-1} F_d + E_d, \quad (28e)$$

$$F := \tilde{C}_s M^{-1} F_d, \quad (28f)$$

$$g := B_d \tilde{A}_s M^{-1} D_d \tilde{g}_s - B_d \tilde{g}_s, \quad (28g)$$

$$h := \tilde{h}_s - \tilde{C}_s M^{-1} D_d \tilde{g}_s. \quad (28h)$$

It is interesting to note that the converter scheme in Fig. 14 can be also used if there are no dynamic elements (inductors and capacitors) into the circuit, i.e. the state dimension is zero and the matrices A_d , B_d , E_d and C_d disappear. Such circuits are typically used to describe basic topologies of power electronics converters, e.g. a single phase full bridge rectifier with diodes, an ideal sinusoidal voltage source and an ideal current source

as a load. These configurations, which can be also part of more complex circuits, cannot be simply modeled and simulated with tools that use switched models of power converters [31].

B. Numerical integration

The switched cone complementarity model (27) can be used for the simulation of the power converter dynamic behavior. In order to obtain the numerical integration of (27), the continuous-time model (27a) can be discretized by using classical techniques for the integration of linear differential equations. For instance, the discretization of (27a) with the backward Euler method leads to

$$x_k = (I - A\theta)^{-1}(x_{k-1} + B\theta z_k + E\theta u_k + g\theta), \quad (29)$$

where k represent the discrete time variable and θ is the sampling period. Moreover the sampled version of (27b) can be written as

$$w_k = q_k + \bar{M}z_k \quad (30)$$

with

$$q_k = C(I - A\theta)^{-1}(x_{k-1} + E\theta u_k + g\theta) + F u_k + h, \quad (31a)$$

$$\bar{M} = D + C(I - A\theta)^{-1}B\theta. \quad (31b)$$

At each time step, given x_{k-1} and u_k , the vector q_k is known and also the state π_k of the externally controlled switches is known. Then one can solve the following *cone complementarity problem*: given q_k , \bar{M} and π_k find z_k such that $\mathcal{C}_{\pi_k}^* \ni z_k \perp w_k \in \mathcal{C}_{\pi_k}$ with w_k given by (30) [13]. Such type of integration algorithm can be simplified so that a lower number of complementarity variables is considered at each integration step. Assume the i th ED is ON. The complementarity variables used for the representation of the OFF characteristic of the ED do not influence the relation between φ and λ (see Fig. 13), then do not affect the converter behavior. The model (19) reduces to

$$\varphi = a_{\text{ON}}\lambda + b_{\text{ON}}^T z_{\text{ON}} + g_{\text{ON}} \quad (32a)$$

$$w_{\text{ON}} = c_{\text{ON}}\lambda + D_{\text{ON}}z_{\text{ON}} + h_{\text{ON}} \quad (32b)$$

with $0 \leq z_{\text{ON}} \perp w_{\text{ON}} \geq 0$. An analogous representation can be obtained from (19) when ED is OFF. Therefore at each step, given the states of the externally controlled EDs, one can select the complementarity representation (5) for the specific ED state (ON or OFF) and use only those matrices in (24). The meaning (and also the size) of the complementarity variables z and w change when external commutations of EDs occur, though φ and λ preserve their physical meanings as current and voltage, or vice versa. By selecting at each step the representations of the EDs corresponding to the ON or OFF states, the original cone complementarity system becomes a linear complementarity system. Then one can compute the matrices (28) and by using (31) solve the following *linear complementarity problem*: given q_k and \bar{M} find z_k such that $0 \leq z_k \perp w_k \geq 0$ (because only constraints in the form (5c) are now considered). The numerical integration is simplified because linear complementarity problems can be efficiently solved [29], [32], [33].

VI. SIMULATION RESULTS

In this section by considering as examples a dc/dc boost converter and a three phase inverter we show the potentialities of the complementarity framework for modeling and simulating power converters.

A. Dc/dc boost converter

Consider the dc/dc boost converter in Fig. 2. From the circuit topology, using (1a)-(1d) the converter can be represented in the form (22a)-(22b) with $x = [x_1 \ x_2]^T$, $u = e$, $\varphi_d = [v_1 \ i_2]^T$, $\lambda_d = [i_1 \ v_2]^T$ and the following matrices

$$A_d = \begin{bmatrix} -\frac{R_1}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_2 C} \end{bmatrix}, B_d = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}, E_d = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \quad (33a)$$

$$C_d = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, D_d = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}, F_d = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \quad (33b)$$

Assuming ED₁ to be an ID one can write

$$\varphi_{s_1} = -\varphi_{d_1} = -z_1, \quad \lambda_{s_1} = \lambda_{d_1} = w_1, \quad (34a)$$

$$0 \leq z_1 \perp w_1 \geq 0. \quad (34b)$$

Assume ED₂ an antiparallel connection of an ID and a electronic switch:

$$\varphi_{s_2} = -\varphi_{d_2} = -z_2, \quad \lambda_{s_2} = \lambda_{d_2} = w_2, \quad (35a)$$

$$\mathcal{K}_\pi^* \ni z_2 \perp w_2 \in \mathcal{K}_\pi, \quad (35b)$$

where $\pi = -1$ if the switch ED₂ is ON and $\pi = 0$ if the switch ED₂ is OFF, see (18). The matrices of the model (23) can be simply obtained from (34a) and (35a); the cones in (27c) will be $\mathcal{C}_\pi^* = \mathbb{R}_+ \times \mathcal{K}_\pi^*$ and $\mathcal{C}_\pi = \mathbb{R}_+ \times \mathcal{K}_\pi$ with $\pi = -1$ if ED₂ is ON and $\pi = 0$ if ED₂ is OFF. Using (28) it is simple to achieve the complementarity representation (27) for the converter under investigation. In particular it will be $A = A_d$, $B = B_d$, $C = C_d$, $D = D_d$, $E = E_d$, $F = F_d$, $g = 0$ and $h = 0$, which can be simply verified to be equal to the model presented in Section II.

Consider the following parameters: $e = 5$ V, $R_1 = 0.1$ Ω , $L = 0.2$ mH, $R_2 = 20$ Ω , $C = 40$ μ F. Moreover an open loop pulse width modulation of ED₂ with a period equal to 100 μ s and a duty cycle equal to 0.5 is considered. Fixed step numerical integrations with different sampling periods have been implemented. At each time step the linear complementarity problem is solved by using the Lemke algorithm [32], which for low order problems is usually faster than the PATH algorithm [33]. Time evolutions of the state variables are depicted in Fig. 16. Similar results are also obtained by using the PLECS tool. Table I shows a comparison of the numerical results assuming the PSpice results as the ‘real’ evolutions. The time required for the complementarity model numerical integration is larger than the time required for the simulation when using PLECS or PSpice. However the integration of the complementarity model is obtained by using standard Matlab code: code optimization and computational burden minimization are out of the scope of this work. The interesting result is that by decreasing the sampling period almost the same rate of improvement is obtained both with PLECS and the integration of the complementarity model. Also, the

comparison with the PSpice simulation results demonstrate the reliability of the complementarity model. The complementarity

TABLE I

COMPARISON OF THE DC/DC BOOST CONVERTER SIMULATION RESULTS.

Sampling period θ	$1 \mu s$	$0.5 \mu s$	$0.1 \mu s$
PSpice simulation time	0.97 s	1.56 s	6.40 s
Compl. simulation time	1.22 s	2.39 s	11.7 s
PLECS simulation time	0.12 s	0.23 s	0.98 s
Compl. rms error	0.067 A 0.18 V	0.033 A 0.088 V	0.0064 A 0.018 V
PLECS rms error	0.060 A 0.20 V	0.030 A 0.098 V	0.0059 A 0.020 V

model can be used to simulate the power converter behavior also in the presence of inconsistent initial conditions. By assuming $x_2(0) = -2$ the simulation results are shown in Fig. 17 and the corresponding error with respect to PSpice in Fig. 17. At the first step the integration of the complementarity model determines the state jump from the inconsistent initial condition to a consistent value of the capacitor voltage [34]. Note that the PLECS simulation is stopped at the first integration step and an error message due to the negative initial capacitor voltage is generated. It should be stressed that for the numerical integration of the power converter complementarity model, differently from the integration techniques that use classical switched models [31], [35], it is not necessary to enumerate and compute the models of the different modes of the converter which are embedded in the complementarity model by means of the constraints on the complementarity variables.

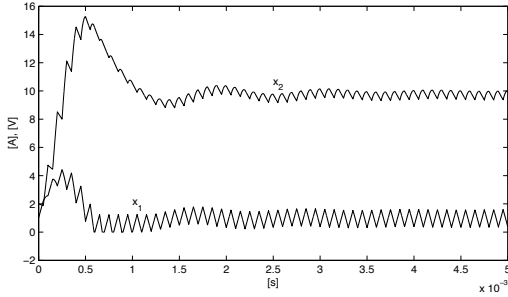


Fig. 16. Inductor current and capacitor voltage starting from $x_1(0) = 1$ A and $x_2(0) = 2$ V.

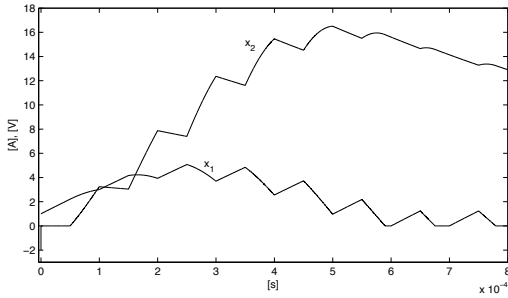


Fig. 17. Inductor current and capacitor voltage with $x_1(0) = 1$ A and $x_2(0) = -2$ V.

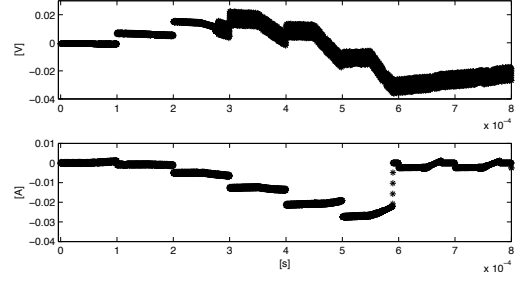


Fig. 18. Voltage (top) and current (bottom) error between the complementarity and the PSpice results.

B. Three phase converter

Consider the three phase converter in Fig. 19. From the circuit topology and using the KVL and KCL after some algebra, by defining $x = [x_C \ x_L \ x_r \ x_s]^T$ (note that $x_t = -x_r - x_s$) and $u = [e \ e_r \ e_s \ e_t]^T$, the converter can be represented in the form (22a)-(22b) with

$$A_d = -\frac{R}{L} \begin{bmatrix} \frac{L}{RR_C C} & -\frac{L}{RC} & 0 & 0 \\ \frac{L}{RL_f} & \frac{LR_f}{RL_f} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \quad (36a)$$

$$B_d = -\frac{1}{3L} \begin{bmatrix} \frac{3L}{C} & \frac{3L}{C} & \frac{3L}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & -1 & -1 \\ 0 & 0 & 0 & -1 & 2 & -1 \end{bmatrix}, \quad (36b)$$

$$E_d = \frac{1}{3L} \begin{bmatrix} 0 & 0 & 0 & 0 \\ \frac{3L}{L_f} & 0 & 0 & 0 \\ 0 & 2 & -1 & -1 \\ 0 & -1 & 2 & -1 \end{bmatrix}, \quad (36c)$$

$$C_d = \begin{bmatrix} -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 1 \end{bmatrix}, \quad (36d)$$

$$D_d = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix}, \quad (36e)$$

and F_d is zero. In order to obtain the comple-

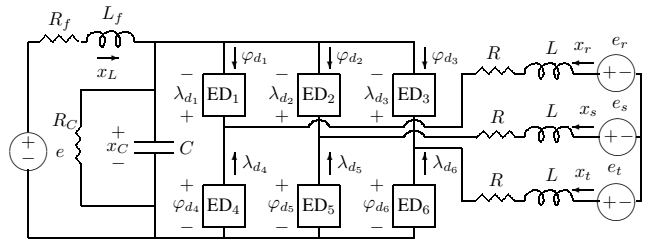


Fig. 19. Three phase power converter with input filter.

mentarity model (27) one must now insert the EDs characteristics. For instance, if the EDs are all IDs, since $\varphi_s = -\varphi_d$ and $\lambda_s = \lambda_d$, by choosing $z = [\varphi_{s_1} \varphi_{s_2} \varphi_{s_3} -\varphi_{s_4} -\varphi_{s_5} -\varphi_{s_6}]^T$ and $w = [-\lambda_{s_1} -\lambda_{s_2} -\lambda_{s_3} \lambda_{s_4} \lambda_{s_5} \lambda_{s_6}]^T$ it is straightforward to obtain the matrices of (20) and using (28) the complementarity representation (27) with $\mathcal{C}_\pi = \mathcal{C}_\pi^* = \mathbb{R}_+^6$.

Note that if the EDs of the converter are modeled as IDs, the resulting matrix $D = D_d$ is skew symmetric, i.e. $D + D^T = 0$. Instead if the EDs are diodes modeled by using the equivalent piecewise-affine characteristic in Fig. 10 it is simple to check that $D + D^T > 0$, whereas $D_d + D_d^T$ is still zero because depends only on the circuit topology and not on the specific EDs characteristics. It is possible to show that for any power converter model the matrix D is skew symmetric when, by considering all converter capacitors (*inductors*) as shortcut (*open circuits*), i.e. with the initial conditions of the corresponding state variables set to zero, there will not exist any dissipation path into the resulting equivalent circuit. If the power diode is represented by means of the equivalent circuit in Fig. 11, independently of the converter in which the diode is included, it will exist at least the dissipation path including R_{ON} and V_B .

Consider the following circuit parameters: $R = 1 \Omega$, $L = 100 \text{ mH}$, $R_f = 2 \Omega$, $L_f = 10 \text{ mH}$, $C_f = 10 \text{ mF}$, $R_C = 10 \text{ k}\Omega$. Moreover consider the inputs $e = 300 \text{ V}$, $e_r = A_e \sin(2\pi f_e t)$, $e_s = A_e \sin(2\pi f_e t - 2\pi/3)$, $e_t = A_e \sin(2\pi f_e t - 4\pi/3)$ with $A_e = 100 \text{ V}$ and $f_e = 48 \text{ Hz}$. The EDs are assumed to be the antiparallel connection of an electronic switch and an ID. A square wave modulation with a frequency of 50 Hz is fixed. Figs. 20-21 report the state variables time evolution. After 0.5 s it is simulated a failure: the third leg is completely disconnected. Such situation is simply simulated by fixing different matrices for the ED models, i.e. open circuits, at the failure time instant. Then at 0.7 s the third phase is connected again. At 1 s a three phase shortcut on the third leg occurs and the first two legs are no more forced, i.e. ED_i for $i = 1, 2, 4, 5$ behave as IDs and for $i = 3, 6$ are shortcuts. The capacitor voltage x_C goes to zero instantaneously and the inductor current goes to $e/R_f = 150 \text{ A}$ with the dynamics of the first order system given by R_f and L_f , see Fig. 22. Note that the (ideal) state discontinuity of the capacitor voltage is simulated without problems by the complementarity model (see [34] for the explicit computation of state discontinuities in switching circuits).

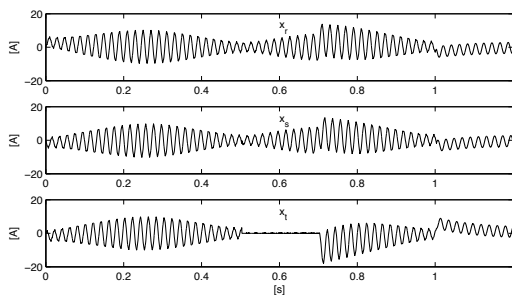


Fig. 20. Currents x_r , x_s and x_t of the three phase converter.

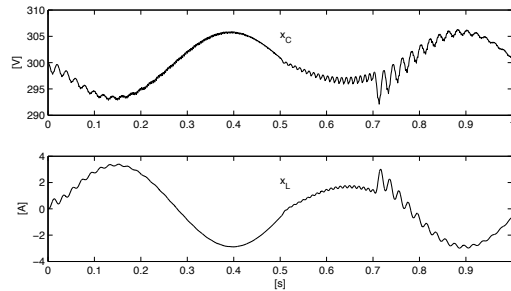


Fig. 21. Capacitor voltage x_C and inductor current x_L of the three phase converter.

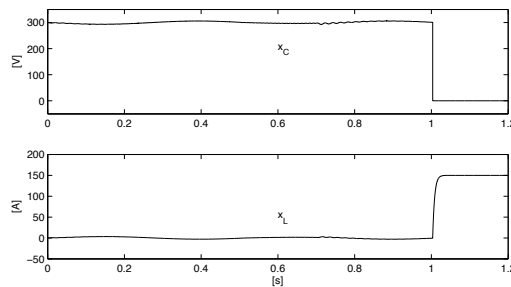


Fig. 22. Capacitor voltage x_C and inductor current x_L of the three phase converter. Note the different vertical time scale with respect to the previous figure.

Up to 0.5 s a performance comparison with the PSpice and PLECS simulations confirm the considerations done for the case of the boost converter results. On the other hand the situations generated at 0.5 s and at 1 s determine inconsistent states which cannot be simulated by using PLECS.

VII. CONCLUSION

Complementarity formalism has been proposed as a framework for representing complete switched model of power converters and for their time-domain analysis. The complementarity model can be constructed without explicitly detailing all modes of the converter and by representing the piecewise-affine current-voltage characteristics of the electronic devices (EDs) at the desired level of abstraction. A general procedure for the construction of the complementarity model has been presented. We have shown that any piecewise-affine relation can be represented by means of an equivalent resistors-diodes-sources (RDS) circuit in which an ideal diode is associated to each change of slope of the characteristic. The RDS circuit allows to determine a static complementarity model of the ED characteristic and the use of ideal switches generalizes the RDS circuits also for EDs with externally controlled commutations. A feedback structure of the converter topology model with the complementarity models of the devices characteristics leads to the final switched cone complementarity model of the power converter. A dc/dc boost converter and a square wave inverter have been presented as examples in order to illustrate the potentialities of the complementarity models for time-domain analysis and for the numerical simulation of power

converters behaviors also in the presence of inconsistent state conditions.

The use of the complementarity formalism opens interesting new frontiers for the modeling and formal analysis of power electronics converters. For instance, by combining the complementarity model with the passivity concept one can prove existence, uniqueness and stability of solutions of power converters. In [36] the complementarity model has been used for computing steady state solutions of a simple converter topology. That could represent the basis for the use of the complementarity framework for frequency-domain analysis of converters, which is a direction of future research. Moreover, the proposed approach can be used for modeling other classes of nonlinear circuits, e.g. sensing circuits containing elements such as thermistor and bridges. On the other hand, although the complementarity formalism is valid also for controlled converters, it is not easy to predict how the complementarity formalism might help for the power converters control design. The main difficulty is that the power converters control acts on the model indexes of the switching set, i.e. the cones at which the complementarity variables belong. Overall, the complementarity framework seems to be useful to tackle, in a future research, a wide range of different topics with practical interest in power electronics.

REFERENCES

- [1] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*, Prentice-Hall, Reading, Massachusetts, 2001.
- [2] D. Maksimovic, A. M. Stankovic, V. J. Thottuvelil, and G. C. Verghese, "Modeling and simulation of power electronic converters", *Proceedings of the IEEE*, vol. 89, no. 6, pp. 898–912, 2001.
- [3] J. M. Burdio and A. Martinez, "A unified discrete-time state-space model for switching converters", *IEEE Trans. on Power Electronics*, vol. 10, no. 6, pp. 694–707, 1995.
- [4] W. P. M. H. Heemels, M. K. Camlibel, A. J. van der Schaft, and J. M. Schumacher, "Modelling, well-posedness, and stability of switched electrical networks", in *Hybrid Systems: Computation and Control*, O. Maler and A. Pnueli, Eds., LNCS 2623, pp. 249–266. Springer, Berlin, 2003.
- [5] J. Sun, D.M. Mitchell, M.F. Greuel, P.T. Krein, and R.M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode", *IEEE Trans. on Power Electronics*, vol. 16, no. 4, pp. 482–492, 2001.
- [6] L. Iannelli, K. H. Johansson, U. Jonsson, and F. Vasca, "Subtleties in the averaging of a class of hybrid systems with applications to power converters", *Control Engineering Practice*, vol. 16, pp. 961–975, 2008.
- [7] A. Ammous, K. Ammous, M. Ayedi, Y. Ounajjar, and F. Sellami, "An advanced PWM-switch model including semiconductor device nonlinearities", *IEEE Trans. on Power Electronics*, vol. 18, no. 5, pp. 1230–1237, 2003.
- [8] J. Chen and K. D. T. Ngo, "Alternative forms of PWM switch models in discontinuous conduction mode", *IEEE Trans. on Aerospace and Electronic Systems*, vol. 37, no. 2, pp. 754–758, 2001.
- [9] M. Di Bernardo and F. Vasca, "Discrete time maps for the analysis of bifurcations and chaos in dc/dc converters", *IEEE Trans. on Circuits and Systems-I*, vol. 47, no. 2, pp. 130–143, 2000.
- [10] L. O. Chua, C. A. Desoer, and E. S. Kuh, *Linear and Nonlinear Circuits*, McGraw-Hill, New York, USA, 1987.
- [11] L. Vandenberghe, B. L. De Moor, and J. Vandewalle, "The generalized linear complementarity problem applied to the complete analysis of resistive piecewise-linear circuits", *IEEE Trans. on Circuits and Systems*, vol. 36, no. 11, pp. 1382–1391, 1989.
- [12] M. K. Camlibel, W. P. M. H. Heemels, A. J. van der Schaft, and J. M. Schumacher, "Switched networks and complementarity", *IEEE Trans. on Circuits and Systems-I*, vol. 50, no. 8, pp. 1036–1046, 2003.
- [13] R. Frasca, *Modeling and Simulation of Switched Electrical Networks: a Complementary Systems Approach*, PhD thesis, Department of Engineering, University of Sannio, Benevento, Italy, 2007.
- [14] F. Vasca, L. Iannelli, and M. K. Camlibel, "A new perspective in power converters modeling: complementarity systems", in *Proc. of the IEEE Power Electronics Specialists Conference*, Orlando, Florida, 2007, pp. 1817–1823.
- [15] F. Yuan and A. Opal, "Computer methods for switched circuits", *IEEE Trans. on Circuits and Systems I-Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1013–1024, 2003.
- [16] P. Pejovic and D. Maksimovic, "A new algorithm for simulation of power electronic systems using piecewise-linear device models", *IEEE Trans. on Power Electronics*, vol. 10, no. 3, pp. 340–348, 1995.
- [17] H. Jin, "Behavior-mode simulation of power electronic circuits", *IEEE Trans. on Power Electronics*, vol. 12, no. 3, pp. 443–452, 1997.
- [18] P. Maffezzoni, L. Codecasa, and D. D'Amore, "Event-driven time-domain simulation of closed-loop switched circuits", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 11, pp. 2413–2426, 2006.
- [19] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*, McGraw-Hill, New York, 1969.
- [20] T. E. Stern, *Piecewise-Linear Network Theory*, PhD thesis, MIT Research Laboratory of Electronics, Cambridge, MA, USA, 1956.
- [21] L. O. Chua, "Nonlinear circuits", *IEEE Trans. on Circuits and Systems*, vol. 31, no. 1, pp. 69–87, 1984.
- [22] L. Iannelli, F. Vasca, and M. K. Camlibel, "Complementarity and passivity for piecewise linear feedback systems", in *Proc. of the IEEE Conference on Decision and Control*, San Diego, California, 2006, pp. 4212–4217.
- [23] M. K. Camlibel, L. Iannelli, and F. Vasca, "Passivity and complementarity", *GRACE Technical Report 352*, University of Sannio, available at www.grace.ing.unisannio.it, 2006.
- [24] N. L chevin, C. A. Rabbath, and C. Dufour, "A digital control perspective for real-time modeling of electrical switching systems", *IEEE Control Systems Magazine*, vol. 25, no. 6, pp. 69–85, 2005.
- [25] M. H. Rashid, Ed., *Power Electronics Handbook*, Academic Press, 2007.
- [26] D. M. W. Leenaerts and W. M. G. van Bokhoven, *Piecewise Linear Modelling and Analysis*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 1998.
- [27] B. De Kelper, L. A. Dessaint, K. Al-Haddad, and H. Nakra, "A comprehensive approach to fixed-step simulation of switched circuits", *IEEE Transactions on Power Electronics*, vol. 17, no. 2, pp. 216–224, 2002.
- [28] A. J. van der Schaft and J. M. Schumacher, "Complementarity modelling of hybrid systems", *IEEE Trans. on Automatic Control*, vol. 43, no. 4, pp. 483–490, 1998.
- [29] F. Vasca, L. Iannelli, M. K. Camlibel, and R. Frasca, "A new perspective in power converter modelling: complementarity systems", *GRACE Technical Report 441*, University of Sannio, available at www.grace.ing.unisannio.it, 2008.
- [30] W.M. Haddad and D.S. Bernstein, "Robust stabilization with positive real uncertainty: beyond the small gain theorem", in *Proc. of the IEEE Conference on Decision and Control*, Honolulu, Hawaii, 1990, pp. 2054–2059.
- [31] J. H. Allmeling and J. H. Hammer, "PLECS - piecewise linear electrical circuit simulation for Simulink", in *Proc. of the IEEE International Conference on Power Electronics and Drive System*, Hong Kong, 1999, pp. 355–360.
- [32] J. E. Lloyd, "Fast implementation of Lemke's algorithm for rigid body contact simulation", in *Proc. of the IEEE International Conference on Robotics and Automation*, Barcelona, Spain, 2005, pp. 4538–4543.
- [33] S. Dirkse, M. C. Ferris, and T. Munson, "The PATH solver", 2008, <http://pages.cs.wisc.edu/~ferris/path.html>.
- [34] R. Frasca, M. K. Camlibel, I. C. Goknar, L. Iannelli, and F. Vasca, "State discontinuity analysis of linear switched systems via energy function optimization", in *Proc. of the IEEE International Symposium on Circuits and Systems*, Seattle, Washington, 2008, pp. 540–543.
- [35] H. S. H. Chung and A. Ioinovici, "Fast computer-aided simulation of switching power regulators based on progressive analysis of the switches' state", *IEEE Trans. on Power Electronics*, vol. 9, no. 2, pp. 206–212, 1994.
- [36] L. Iannelli and F. Vasca, "Computation of limit cycles and forced oscillations in piecewise linear feedback systems through a complementarity approach", in *Proc. of the IEEE Conference on Decision and Control*, Cancun, Mexico, 2008.